Te1120

PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10082055	02/26/2002	~~345~~ 702	117	~~2173~~ 2857	Raymond

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**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2001-269216 09/05/2001

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed ☐ yes ☐ no 35 USC 119 conditions met ☐ yes ☐ no Verified and Acknowledged Examiners's intials			ATTORNEY DOCKET NO 100021-00072

TITLE : Test circuit and semiconductor integrated circuit effectively carrying out verification of connection of nodes

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg. / Print Fig.	Application Examiner
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